## **CLAIMS**

## What is Claimed is:

- 1. A semiconductor device comprising:
- 5 a semiconductor layer including an element formation region;
  - a trench isolation surrounding the element formation region of the semiconductor layer; and

a coating film having the property of suppressing passage of oxygen, said coating film covering at least a portion of the trench isolation and a portion of the element formation region astride the border between the trench isolation and the element formation region.

- The semiconductor device of Claim 1, wherein
   the coating film directly contacts the semiconductor layer.
- 3. The semiconductor device of Claim 1, further comprising an element including: source/drain regions provided in the element formation region of the semiconductor

layer;

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- a gate dielectric formed by thermally oxidizing the top of the element formation region of the semiconductor layer; and
  - a gate electrode provided on the gate dielectric.
- 20 4. The semiconductor device of Claim 3, wherein the element is an n-type MISFET.
  - 5. The semiconductor device of Claim 1, wherein the coating film is formed of silicon nitride.
  - 6. The semiconductor device of Claim 1, wherein
- a plurality of the element formation regions are provided, and

the coating film covers the top of the trench isolation and extends to the tops of the two element formation regions of the semiconductor layer adjacent to the trench isolation.

- 7. The semiconductor device of Claim 1, wherein
  a depression is provided in the upper edge of the trench isolation, and
  the coating film extends from the bottom of the depression to the top of the elemen
- the coating film extends from the bottom of the depression to the top of the element formation region.
- 5 8. A method for fabricating a semiconductor device comprising the steps of:
  - (a) forming a trench isolation surrounding an element formation region in a semiconductor layer;
  - (b) forming a coating film having the property of suppressing passage of oxygen to lie from the top of the semiconductor layer to the top of the trench isolation; and
- (c) removing a portion of the coating film to form a partial coating film that covers at least a portion of the trench isolation and a portion of the element formation region of the semiconductor layer astride the border between the trench isolation and the element formation region.
  - 9. The method for fabricating a semiconductor device of Claim 8, further comprising the steps of:
  - (d) thermally oxidizing an upper part of the element formation region of the semiconductor layer after the step (c) to form a gate dielectric;
    - (e) forming a gate electrode on the gate dielectric; and

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- (f) forming source/drain regions in the element formation region by using the gate electrode as a mask.
  - 10. The method for fabricating a semiconductor device of Claim 8, wherein in the step (b), the coating film is formed of silicon nitride.
  - 11. A method for fabricating a semiconductor device comprising the steps of:
- (a) forming a trench isolation surrounding an element formation region in a25 semiconductor layer;
  - (b) forming a mask having an opening allowing the top of the trench isolation and the top of a portion of the element formation region adjacent to the trench isolation to be

exposed;

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- (c) forming, on the mask, a coating film covering the sides and the bottom of the opening and having the property of suppressing passage of oxygen;
- (d) removing an upper part of the mask and an upper part of the coating film to form a partial coating film that covers a portion of the trench isolation and a portion of the element formation region astride the border between the trench isolation and the element formation region; and
  - (e) removing the remaining mask.
- 12. The method for fabricating a semiconductor device of Claim 11, further comprising the steps of:
  - (f) thermally oxidizing an upper part of the element formation region of the semiconductor layer after the step (e) to form a gate dielectric;
    - (g) forming a gate electrode on the gate dielectric; and
- (h) forming source/drain regions in the element formation region by using the gateelectrode as a mask.
  - 13. The method for fabricating a semiconductor device of Claim 11, wherein in the step (a), a depression is formed in the upper edge of the trench isolation, and in the step (d), the partial coating film is formed to extend from the bottom of the depression to the top of the element formation region.
- 20 14. The method for fabricating a semiconductor device of Claim 11, wherein in the step (c), the coating film is formed of silicon nitride.